This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Please amend claim 1 as follows.

1. (Currently amended) In an integrated circuit having a substrate and a plurality of stacked metal layers thereover, said metal layers delineated as interconnections for said integrated circuit, a **[high density]** capacitor structure between adjacent stacked metal layers comprising:

a portion of a first selected one of said stacked metal layers and a portion of a second selected one of said stacked metal layers, said second selected stacked metal layer portion above and adjacent said first selected stacked metal layer portion;

a first capacitor dielectric layer over said first selected stacked metal layer portion;

a first capacitor metal plate layer over said first capacitor dielectric layer;

a second capacitor dielectric layer under said second selected stacked metal layer portion;

a second capacitor metal plate layer under said second **[capacitor dielectric layer]** selected stacked metal layer portion and over and **[extending]** spaced from said first capacitor metal plate layer; and

a metal capacitor via layer between and connecting said first capacitor metal plate layer and said second capacitor metal plate layer, said metal capacitor via layer forming a first terminal of said capacitor structure; and

a first via connecting said first selected stacked metal layer portion and said second selected stacked metal layer portion to form a second terminal of said capacitor structure.

2. (Original) The integrated circuit of claim 1 wherein at least one of said first or second stacked metal layers comprises a plurality of stacked, contiguous metal layers of differing composition.

3. (Original) The integrated circuit of claim 1 wherein said first capacitor dielectric layer and said first capacitor metal plate layer are laterally co-extensive.

4. (Original) The integrated circuit of claim 1 wherein said second capacitor dielectric layer and said second capacitor metal plate layer are laterally co-extensive.

5. (Original) The integrated circuit of claim 4 wherein said first capacitor dielectric layer, said first capacitor metal plate layer, said second capacitor dielectric layer and said second capacitor metal plate layer are laterally co-extensive.

6. (Original) The integrated circuit of claim 1 wherein said metal capacitor via layer is connected to another portion of said second selected stacked metal layer to form a connection to said second capacitor structure terminal.

7. (Original) The integrated circuit of claim 1 further comprising a metal layer laterally co-extensive with said first capacitor dielectric layer and said first capacitor metal plate layer, and arranged between said first capacitor dielectric layer and said first selected stacked metal layer portion so that said metal layer forms a plate for said first capacitor.

8. (Original) The integrated circuit of claim 1 further comprising a metal layer laterally co-extensive with said second capacitor dielectric layer and said second capacitor metal plate layer, and arranged between said second capacitor dielectric layer and said second selected stacked metal layer portion so that said metal layer forms a plate for said second capacitor.